



Introducing the Cupria™ 5101a

testing & evaluation module for the rm-CDS6000 Development System



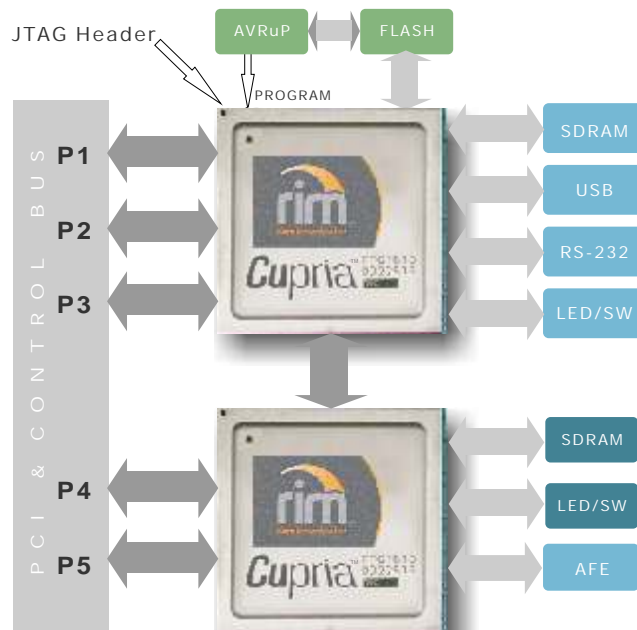
The Cupria™ 5101a is a PTMC line card providing high performance implementation of the Cupria™ IPSL data pump for the evaluation and development of IPSL-based applications. The Cupria™ 5101a can interface to a PCI 32/33 or a PCI 64/66 bus and offers various interfaces, fast on-board memory resources and two Cupria™ FPGAs. The Cupria™ 5101a is mechanically and electrically compliant to the standard PTMC specifications.

The FPGA device interfaces to four 64-pin connectors on the motherboard. It serves as a base for a daughter card and offers I/O diversity to the Cupria™ 5101a such as GigE or T1/E1.

The FPGA design incorporates two Cupria™ FPGA devices with a combined gate count well over 200,000 gates. The two FPGA devices interface to the various peripheral on the Cupria™ 5101a as shown in the block diagram below. They also interconnect to each other via general purpose pins and clock pins for co-operative development.

Firmware and Software

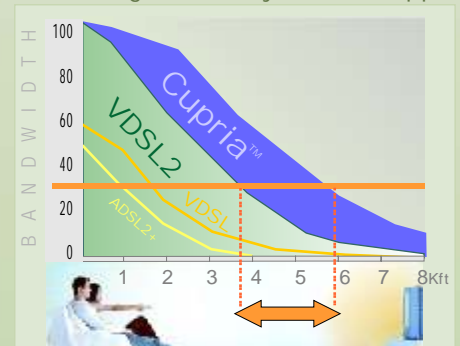
- Provides a package of binary executable software for evaluation of Cupria™ IPSL along with lower level libraries for related development work using the FPGAs.
- An API library is supplied which provides an interface to the core firmware onboard the FPGA devices.



Cupria™ is the only xDSL chipset optimized to meet the rigorous demand of high-fidelity IP over copper

- Enhanced QoS - Cupria™ supports 4 discrete SLA's compared to only two for VDSL2 - significantly reducing packet loss for IPTV networks.
- Four priority levels supports discrete video, VoIP, data, and IGMP queuing streams to deliver superior voice and video quality.
- Inter-frame preemptive bit queuing allows a mix of contending SLA's within single DSL frames to increase transport efficiency.
- Cupria's™ R-QAM multitone modulation efficiently uses every hertz of the copper spectrum, yet requires far fewer tones to achieve faster synching and higher payload ratios with lower bit-error rates than VDSL2.
- Longer copper reach serves 30 to 40% larger distribution area than VDSL2 - cutting IPTV access network costs significantly.

Delivering Hi-Fidelity IP over Copper



30 - 40% GREATER RATE & REACH

for more information, please refer to www.rimsemi.com member IPSLsig™



Key Features

- TR-69 compliant
- Triple-Play over pure IP transport
- Advanced R-QAM Encoding / Decoding minimizes Bit Error Rates
- Enhanced QOS with grooming at the CPE optimizes HDTV quality
- Capable of Symmetric or Asymmetric, with up to 95% of bandwidth available for downstream video (cable-competitive HDTV)
- Improved Signal-to-Noise Tolerance
- -150 dBm/Hz front-end noise floor adaptation
- Dynamic Rate Re-partitioning preserves QOS for voice, video, & data
- PSD shaping for maximum copper efficiency
- Region-specific RFI notching
- Adaptive signal-to-noise ratios
- Short symbol/frame lengths minimizes packet retransmission delays

Development Support

- Reference Designs
- Application Notes
- Installation & User Guide
- Engineering Support

Cupria is Rim Semi's implementation of IPSL™: an advanced xDSL transport protocol designed to outperform current VDSL2 technology. For more information on Internet Protocol Subscriber Line (IPSL™) email info@IPSLsig.org.



Cupria™ 5101a Line Card Specifications

Embedded Processor

Several different processor cores are available for both FPGA devices. These cores can be used to execute C-based algorithms and control the logic resources implemented in the FPGA. Either an Altera NIOS II processor core, or other open-source processor core designs may be utilized.

Peripherals

- **Memory:** The FPGAs are connected to up to 256Mbytes of SDRAM with a 16/32 bit data bus width, available to the embedded processor core or as memory buffers.
- **PCI Interface:** Interfaces directly to the PCI bus via the industry standard PTMC J11, J12 and J13 connectors. An embedded PCI core is used to communicate over the PCI bus with the host system on the motherboard.
- **FLASH Storage:** The FPGA firmware is stored onboard in an up to 256Mbit serial flash device. The flash device is partly used to store the configuration for both FPGAs, and also to hold program code for the onboard processors.
- **AVR Device:** An Atmel AVR device is present on board to interface between the flash device and the FPGA devices. The AVR is used to program and read the flash.
- **Embedded JTAG** for configuration and downloading.

Power Requirements

Power is supplied to the Cupria™ 5101a via the PTMC connectors. Several AC-DC converters generate the appropriate voltage rails for the different devices and interfaces present on board. Optionally, the Cupria™ 5101a can be used as a stand alone module and is powered via the external power connector.

Form Factor

The individual Cupria™ 5101a boards are based on the industry standard, (74mm x 149mm) PTMC form factor with interconnects J11-J14.

Hardware and software features discussed here are subject to change without notice. Actual product features could differ materially from expectation for reasons including but not limited to following: product development difficulties, market demand and acceptance of products, the impact of changing economic conditions, business conditions in the Internet and telecommunications industries, reliance on third parties, including potential suppliers, licensors, and licensees. Rim Semiconductor is under no obligation to revise or update any statement in order to reflect events or circumstances that may arise in the future. Cupria™ 5101 pb rel061507 1